WHAT IS CLAIMED IS:

1. A semiconductor device with a CMOS transistor comprising:

a plurality of gate electrodes arranged in parallel with one another;

an n-channel MOS region and a p-channel MOS region of said CMOS transistor which are arranged adjacent to each other in a lengthwise direction of said plurality of gate electrodes; and

a wire for connecting said n-channel MOS region and said p-channel MOS region,

wherein said wire has a width greater than a distance between every two adjacent ones of said plurality of gate electrodes, and

a portion of said wire is disposed right above a portion of said gate electrode with an insulating film interposed therebetween.

2. The semiconductor device according to claim 1,

wherein said insulating film is formed on a top face and a side face of said gate electrode, and

said wire is buried in a first opening formed by carrying out etching on an interlayer insulating film which is deposited on said insulating film and is made of a material different from a material for said insulating film.

3. The semiconductor device according to claim 2,

wherein said wire is further buried in a second opening formed in said insulating film, to be electrically connected to said gate electrode.

4. The semiconductor device according to claim 3,

wherein said first opening and said second opening form one opening which provides a shape having six corners or more in said interlayer insulating film in plan view.

5. A method of manufacturing a semiconductor device with a CMOS transistor, comprising the steps of:

forming a plurality of gate electrodes so as to be arranged in parallel with one another on a semiconductor substrate;

forming an insulating film on a top face and a side face of said gate electrode;

forming an interlayer insulating film made of a material different from a material for said insulating film, on said insulating film;

carrying out etching on said interlayer insulating film using said insulating film as an etch stop layer, to form a first opening having a width greater than a distance between every two adjacent ones of said plurality of gate electrodes;

depositing a metal film on said interlayer insulating film; and

removing said metal film on said interlayer insulating film, except a portion of said metal film which is buried in said first opening.

6. The method of manufacturing a semiconductor device according to claim 5, further comprising a step of:

etching a portion of said insulating film which is exposed after said first opening is formed, to form a second opening.

7. The method of manufacturing a semiconductor device according to claim

5,

wherein said metal film on said interlayer insulating film except said portion of said metal film which is buried in said first opening is removed by etch back.

5